WHAT IS CLAIMED IS:

1. An array substrate for in-plane switching liquid crystal display device, comprising:

a gate line arranged in a first direction on a substrate;

a data line arranged in a second direction perpendicular to the gate line, the data line define a pixel region with the gate line;

a plurality of common electrodes located in the pixel region and arranged in the second direction;

a common line arranged in the first direction and connected to the pluarity of common electrodes;

a plurality of pixel electrodes located in the pixel region and arranged in the second direction, the plurality of pixel and common electrodes having at least one bent portion; and

a plurality of light-shielding patterns between one end of the pixel electrode and the intersection of the common line and at least one common electrode.

2. The array substrate of claim 1, further comprising a thin film transistor that is connected to the gate line and the dat line.

3. The array substrate of claim 2, wherein the thin film transistor includes a gate electrode, a source electrode and a drain electrode.

4. The array substrate of claim 3, further comprising a pixel connecting line that extends from the drain electrode and is connected to the plurality of pixel electrodes.

5. The array substrate of claim 4, wherein the pixel connecting line is disposed at the end of the common electrode.

6. The array substrate of claim 5, wherein the pixel connecting line is overlapped by the end of at least one common electrode.

7. The array substrate of claim 1, wherein the plurality of light-shielding patterns are the same material as the data line.

8. The array substrate of claim 1, wherein each light-shielding pattern is disposed at an acute angle area where each common electrode forms an acute angle with the common line.

9. The array substrate of claim 1, wherein each light-shielding pattern is disposed between an acute angle, where each common electrode forms an acute angle with the common line, and the end of each pixel electrode.

10. The array substrate of cliam 1, wherein the plurality of pixel and common electrodes are arranged in an alternating manner with a predetermined interval between adjacent pixel and common electrodes

11. The array substrate of claim 1, further comprising a capacitor electrode that is overlapped by the common line.

12. The array substrate of claim 11, wherein the capacitor electrode is made of the same material as the data line.

13. The array substrate of claim 11, wherein the capacitor electrode is connected to at least one pixel electrode.

14. The array substrate of claim 11, wherein the capacitor electrode is connected to the plurality of light-shielding patterns.

15. The array substrate of claim 1, wherein one of the plurality of common electrodes extends over an adjacent pixel region.

16. The array substrate of claim 1, wherein the plurality of common and pixel electrodes has a substantially zigzag shape.

17. The array substrate of claim 1, wherein the data line has a substantially zigzag shape.

18. The array substrate of claim 1, wherein a portion of the data line is overlapped by a portion of the adjacent common electrode.

19. A method of forming an array substrate for an in-plane switchng liquid crystal display device, comprising:

forming a gate line and a gate electrode on a substrate;

forming a gate insulation layer on the substrate to cover the gate line and the gate electrode;

forming a semiconductor layer on the gate insulation layer;

forming a source electrode and a drain electrode on the semiconductor layer and simultaneously forming a data line, a pixel connecting line and a plurality of light-shielding patterns on the gate insulation layer, thereby defining an intermediate structure;

forming a passivation layer over the substrate to cover the intermediate structure, the passivation layer having a plurality of contact holes; and

forming a common electrode and a plurality of common and pixel electrodes on the passivation layer, the plurality of common and pixel electrodes having a substantially zigzag shape.

20. The method of claim 19, wherein each light-shielding pattern is disposed between one end of the pixel electrode and the intersection of the common line and at least common electrode.

21. The method of claim 19, further comprising forming a capacitor electrode when forming the data line.

22. The method of claim 21, wherein the capacitor electrode is overlapped by the common line.

23. The method of claim 22, wherein the capacitor electrode is connected to the plurality of light-shielding patterns.

24. The method of claim 19, wherein one of the light-sheilding patterns is connected to one of the pixel electrodes through one of the contact holes.

25. The method of claim 19, wherein the data line has a substantially zigzag shape.

26. The method of claim 19, wherein a portion of the data line is overlapped by a portion of the adjacent common electrode.

27. The method of claim 19, wherein the semiconductor layer sequentially includes an active layer and an ohmic contact layer over the gate electrode.

28. The method of claim 19, wherein the gate line is arranged in a first direction and is connected to the gate electrode.

29. The method of claim 19, wherein the data line is arranged in a second direction perpendicular to the gate line.

30. The method of claim 29, wherein the source electrode extends from the data line.

31. The method of claim 19, wherein the drain electrode extends from the pixel connecting line.

32. The method of claim 19, wherein each pixel electrode is connected to the pixel connecting line through each contact hole.

33. A method of forming an array substrate for an in-plane switchng liquid crystal display device, comprising:

forming a gate line arranged in a first direction on a substrate;

forming a data line arranged in a second direction perpendicular to the gate line, the data line define a pixel region with the gate line;

forming a plurality of common electrodes located in the pixel region and arranged in the second direction;

forming a common line arranged in the first direction and connected to the pluarity of common electrodes;

forming a plurality of pixel electrodes located in the pixel region and arranged in the second direction, the plurality of pixel and common electrodes having at least one bent portion; and

forming a plurality of light-shielding patterns between one end of the pixel electrode and the intersection of the common line and at least one common electrode.

34. The method of claim 33, further comprising forming a thin film transistor that is connected to the gate line and the dat line.

35. The method of claim 34, wherein the thin film transistor includes a gate electrode, a source electrode and a drain electrode.

36. The method of claim 35, further comprising forming a pixel connecting line that extends from the drain electrode and is connected to the plurality of pixel electrodes.

37. The method of claim 36, wherein the pixel connecting line is disposed at the end of the common electrode.

38. The method of claim 37, wherein the pixel connecting line is overlapped by the end of at least one common electrode.

39. The method of claim 33, wherein the plurality of light-shielding patterns are the same material as the data line.

40. The method claim 33, wherein each light-shielding pattern is disposed at an acute angle area where each common electrode forms an acute angle with the common line.

41. The method of claim 33, wherein each light-shielding pattern is disposed between an acute angle, where each common electrode forms an acute angle with the common line, and the end of each pixel electrode.

42. The method of claim 33, wherein the plurality of pixel and common electrodes are arranged in an alternating manner with a predetermined interval between adjacent pixel and common electrodes.

43. The method of claim 33, further comprising forming a capacitor electrode that is overlapped by the common line.

44. The method of claim 43, wherein the capacitor electrode is made of the same material as the data line.

45. The method of claim 43, wherein the capacitor electrode is connected to at least one pixel electrode.

46. The method of claim 43, wherein the capacitor electrode is connected to the plurality of light-shielding patterns.

47. The method of claim 33, wherein one of the plurality of common electrodes extends over the adjacent pixel region.

48. The method of claim 33, wherein the plurality of common and pixel electrodes has a substantially zigzag shape.

49. The method of claim 33, wherein the data line has a substantially zigzag shape.

50. The method of claim 33, wherein a portion of the data line is overlapped by a portion of the adjacent common electrode.